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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,620	11/01/2003	Fusao Ishii	FIshii001	9893

7590 09/21/2007

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EXAMINER	
THOMAS, BRANDI N	
ART UNIT	**PAPER NUMBER**
2873	
MAIL DATE	**DELIVERY MODE**
09/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/698,620	ISHII, FUSAO	
	Examiner	Art Unit	
	Brandi N. Thomas	2873	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) ____ is/are withdrawn from consideration.

5)☐ Claim(s) ____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) ____ is/are objected to.

8)☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. ____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. ____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *Detailed Action*.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-51 are rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al. (US 2004/0125347).

Regarding claim 1, Patel et al. discloses, in figures 2 and 3A, an electromechanical micromirror device (200), comprising: a single substrate (202) with a lst surface and a second surface; control circuitry (not shown, figure 2 shows the second surface of the device substrate) disposed on said lst surface of said single substrate, and a micromirror section (215) disposed on said second surface of said single substrate, wherein said micromirror section (215) comprises: a micromirror (201), and at least one support structure (230) for supporting said micromirror (201) (section 0047, lines 6-13).

Regarding claims 2 and 35, Patel et al. discloses, in figures 2 and 3A, an electromechanical micromirror device (200), wherein said control circuitry comprising a circuit selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor

circuits, organic transistor circuits, and conjugated polymer transistor circuits (section 0043, lines 7-8).

Regarding claims 3, 19, and 36, Patel et al. discloses, in figures 2 and 3A, an electromechanical micromirror device (200), wherein said single substrate (201) comprising a substrate selected from the group consisting of a silicon-on-insulator (SOI) substrate, a silicon substrate, polycrystalline silicon substrate, glass substrate, plastic substrate, ceramic substrate, germanium substrate, SiGe substrate, SiC substrate, sapphire substrate, quartz substrate, GaAs substrate, and an InP substrate (section 0047, line 8).

Regarding claims 4, 20, and 37, Patel et al. discloses, in figures 2, 3A, and 4C, an electromechanical micromirror device (200), wherein said micromirror section (215) additionally comprises at least 1addressing electrode (283) for actuating said micromirror (201) (section 0047, lines 16-18).

Regarding claims 5, 21, and 38, Patel et al. discloses, in figures 2, 3A, and 3C, an electromechanical micromirror device (200), additionally comprising at least one electrically conductive routing line (213) integral with said single substrate (202) that connects said control circuitry to said at least 1addressing electrode (283) (section 0049, lines 6-7 of first column and lines 19-30 of second column).

Regarding claims 6, 22, and 39, Patel et al. discloses, in figures 2, 3, and 4C, an electromechanical micromirror device (200), wherein said at least one electrically conductive routing line (213)comprises a via through said single substrate (202) and a metallization in said via (section 0049, lines 6-7 of first column and lines 19-30 of second column).

Regarding claims 7, 23, and 40, Patel et al. discloses, in figure 6B, an electromechanical micromirror device (200), wherein said single substrate (202) additionally comprises an insulating layer (301and 307) between said first surface and said second surface (section 0069, lines 4-5).

Regarding claims 8, 24, and 41, Patel et al. discloses, in figures 2 and 3A-3C, an electromechanical micromirror device (200), wherein said micromirror (201) is a metallic mirror (section 0058, lines 5-9).

Regarding claims 9, 25, and 42, Patel et al. discloses, in figures 2 and 3A-3C, an electromechanical micromirror device (200), wherein said micromirror (201) is a multilayer dielectric mirror (section 0058, lines 5-9).

Regarding claims 10 and 26, Patel et al. discloses, in figures 2 and 3A-3C, an electromechanical micromirror device (200), wherein said micromirror (201) further comprising a substantially planar reflective side (210) with neither recesses nor protrusions (figure 2).

Regarding claims 11, 27, and 46, Patel et al. discloses, in figures 2-6B, an electromechanical micromirror device (200), wherein said micromirror (201) comprising a reflective surface (210) having no edges perpendicular to a projection direction of an incident light propagation vector onto said single substrate (202) (section 0012, lines 7-12) (figures 2-6).

Regarding claims 12, 28, and 47, Patel et al. discloses, in figure 2, an electromechanical micromirror device (200), wherein said reflective surface (210) of said micromirror (201) further comprising a polygon-shaped reflective surface (section 0049, lines 16-24).

Regarding claims 13, 29, and 48, Patel et al. discloses, in figure 2, an electromechanical micromirror device (200), wherein said polygon-shaped reflective surface (210) is selected from

the group consisting of a rectangle-shaped reflective surface and a hexagon-shaped reflective surface (section 0049, lines 16-24).

Regarding claims 14, 30, and 49, Patel et al. discloses, in figures 2, 3A, and 3B, an electromechanical micromirror device (200), wherein said micromirror section additionally comprises: a torsion hinge (230) disposed underneath and supporting said micromirror support structure (251), and a said torsion hinge (230) further comprising a pair of supporting structures (251) for supporting said torsion hinge (230) on said substrate (201) (section 0050, lines 3-7).

Regarding claims 15, 31, and 50, Patel et al. discloses, in figures 2, 3A, and 3B, an electromechanical micromirror device (200), wherein said micromirror section (215) additionally comprises at least one stopping member (255) for limiting the rotation of said micromirror (201) (section 0050, lines 10-15).

Regarding claims 16, 32, and 51, Patel et al. discloses, in figures 2, 3A, and 3B, an electromechanical micromirror device (200), wherein said at least one stopping member (255) comprises: a lst stopping member (255) for limiting the rotation of said micromirror (201) in a lst direction, and a second stopping member (255) for limiting the rotation of said micromirror in a direction opposite to said lst direction (section 0050, lines 10-19).

Regarding claim 17, Patel et al. discloses, in figures 2 and 3A, an array of electromechanical micromirror device (200) comprising: a single substrate (202) with a 1st surface and a 2nd surface; a control circuitry (not shown, figure 2 shows the second surface of the device substrate) disposed on said lst surface of said substrate, and an array micromirror sections (215) disposed on said 2nd surface of said substrate, wherein said micromirror section (215)

comprises a micromirror (201), and a support structure (230) for supporting said micromirror (201) (section 0047, lines 6-13 and 0048, lines 1-6).

Regarding claim 18, Patel et al. discloses, in figures 2 and 3A, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a one-dimensional or 2- dimensional array (section 0053), wherein said control circuitry comprising a circuit selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistor circuits (section 0043, lines 5-9).

Regarding claim 33, Patel et al. discloses, in figures 2 and 3A, a spatial light modulator (SLM) (section 0045, lines 1-2) comprising an array of electromechanical micromirror device (200), comprising: a single substrate (202) with a lst surface and a second surface; a control circuitry (not shown, figure 2 shows the second surface of the device substrate) disposed on said lst surface of said single substrate, and an array micromirror section (201) disposed on said second surface of said single substrate, wherein said micromirror section (215) comprises: a micromirror (201), and a support structure (230) for supporting said micromirror (201) (section 0047, lines 6-13).

Regarding claim 34, Patel et al. discloses, in figures 2 and 3A, a method of fabricating an array of electromechanical micromirrors (200), comprising the steps of: providing a single substrate (202) with a lst surface and a second surface; forming control circuitry (not shown,

figure 2 shows the second surface of the device substrate) on said lst surface of said single substrate, and forming a plurality of support structures (230) on said second surface of said single substrate (202) and forming a plurality of micromirrors (215) on top of and supported by said support structures (230) (section 0047, lines 6-13 and 0048, lines 1-6).

Regarding claim 43, Patel et al. discloses, in figures 5B and 5C, a method of fabricating an array of electromechanical micromirror devices (200), wherein said step of forming said micromirrors comprises the steps of: forming said plurality of micromirror support structures (230) embedded in a sacrificial layer (sections 0011, lines 1-10, 0013, lines 3-6, and 0062, lines 5-7), planarizing a top surface of said sacrificial layer and said micromirror support structures (230) (sections 0011, lines 1-10, 0013, lines 3-6, and 0062, lines 5-7), depositing a micromirror material on said top surface (section 0062, lines 5-10); patterning said micromirror material to form a plurality of micromirrors (section 0068, lines 1-12), and removing said sacrificial layer by an etching process (section 0063, lines 1-4 and 0068, lines 1-12).

Regarding claim 44, Patel et al. discloses, in figures 5B and 5C, a method of fabricating an array of electromechanical micromirror devices (200), wherein said step of forming said microstructures in said sacrificial layer further comprising a step of forming said microstructures in a layer composed of a material selected from the group consisting of a photoresist polymer, a silicon oxide, a silicon nitride, a silicon oxynitride, and an amorphous silicon (section 0062, lines 15-18).

Regarding claim 45, Patel et al. discloses, in figures 5B and 5C, a method of fabricating an array of electromechanical micromirror devices (200), wherein said planarizing step of

planarizing said top surface further comprising a step of applying a chemical mechanical polishing (CMP) process (section 0062, lines 18-27).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 52-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. (US 2004/0125347) in view of Chiu et al. (6639713 B2).

Regarding claim 52, Patel et al. discloses a method of fabricating an array of electromechanical micromirrors, comprising the steps of: forming control circuitry (not shown, figure 2 shows the second surface of the device substrate); forming a plurality of support structures (230) followed by forming a plurality of micromirrors (201) on top of and supported by said support structures (230) (sections 0047, lines 6-13 and 0048, lines 1-6) except that it does not show providing a silicon-on-insulator substrate with an epitaxial top silicon layer, an insulator layer, and a bottom silicon layer forming control circuitry on said epitaxial top silicon layer, removing said bottom silicon layer, thereby exposing the insulator layer. Chiu et al. shows that it is known to provide a silicon-on-insulator substrate with an epitaxial top silicon layer (321), an insulator layer (323), and a bottom silicon layer (324) on said epitaxial top silicon layer, removing said bottom silicon layer, thereby exposing the insulator layer for at least partially intercepting a light beam propagating along a beam path (col. 15, lines 51-53 and col.

21, lines 37-52). Therefore it would have been obvious to some1of ordinary skill in the art at the time the invention was made to combine the device of Patel et al. with the silicon-on-insulator substrate of Chiu et al. for the purpose of at least partially intercepting a light beam propagating along a beam path (col. 15, lines 51-53 and col. 21, lines 37-52).

Regarding claim 53, Patel et al. discloses, in figures 6A-6H, a method of fabricating an array of electromechanical micromirror devices, wherein said step of forming said control circuitry comprises a step of fabricating said control circuits selected from a group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar transistor circuits, BiCMOS circuits, and DMOS circuits (section 0043, lines 7-8).

Regarding claim 54, Patel et al. discloses a method of fabricating an array of electromechanical micromirror devices, including a step of removing said bottom silicon layer but does not specifically disclose removing the bottom silicon layer by backgrinding. However, it would have been obvious to 1having ordinary skill in the art at the time the invention was made to use the process of backgrinding for the purpose of ensuring the eradication of the silicon layer on the substrate.

Regarding claim 55, Patel et al. discloses, in figures 6A-6H, a method of fabricating an array of electromechanical micromirror devices, wherein said step of removing said bottom silicon layer comprises a step of applying a chemical mechanical polishing (CMP) step to remove bottom silicon layer (section 0062, lines 18-27).

Regarding claim 56, Patel et al. discloses, in figures 6A-6H, a method of fabricating an array of electromechanical micromirror devices, additionally comprises a step of forming a

plurality of addressing electrodes (283) for actuating said plurality of micromirrors (201) (section 0049, lines 6-7 of first column and lines 19-30 of second column).

Regarding claim 57, Patel et al. discloses, in figures 2, 3A, and 6A-6H, a method of fabricating an array of electromechanical micromirror devices, additionally comprising a step of forming a plurality electrically conductive routing lines (213) integrated with said single substrate (202) for connecting said control circuitry to said plurality of addressing electrodes (283) (section 0049, lines 6-7 of first column and lines 19-30 of second column).

Regarding claim 58, Patel et al. discloses, in figures 2, 3, and 4C, an electromechanical micromirror device (200), wherein said step of forming said plurality of electrically conductive routing lines (213) comprises the steps of: forming at least one via through said substrate (202) and forming a metallization in said via (section 0049, lines 6-7 of first column and lines 19-30 of second column).

Regarding claim 59, Patel et al. discloses, in figures 5B and 5C, a method of fabricating an array of electromechanical micromirror devices (200), wherein said step of forming said micromirrors comprises the steps of: forming said plurality of micromirror support structures (230) embedded in a sacrificial layer (sections 0011, lines 1-10, 0013, lines 3-6, and 0062, lines 5-7), planarizing a top surface of said sacrificial layer and said micromirror support structures (230) (sections 0011, lines 1-10, 0013, lines 3-6, and 0062, lines 5-7), depositing a micromirror material on said top surface (section 0062, lines 5-10); patterning said micromirror material to form a plurality of micromirrors (section 0068, lines 1-12), and removing said sacrificial layer by an etching process (section 0063, lines 1-4 and 0068, lines 1-12).

Regarding claim 60, Patel et al. discloses, in figures 5B and 5C, a method of fabricating an array of electromechanical micromirror devices (200), wherein said planarizing step of planarizing said top surface further comprising a step of applying a chemical mechanical polishing (CMP) process (section 0062, lines 18-27).

Response to Arguments

5. Applicant's arguments filed 1/26/05 have been fully considered but they are not persuasive. Applicant argues that the amended claims now include a single substrate rather than a device substrate. However, Patel discloses a single substrate (202) (section 0047 and figure 2).

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandi N. Thomas whose telephone number is 571-272-2341. The examiner can normally be reached on Monday - Thursday from 6-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Mack can be reached on 571-272-2333. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brandi N Thomas
Examiner
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BNT
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Ricky Mack
RICKY MACK
SUPERVISORY PATENT EXAMINER